



LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY

Approved by AICTE & Permanently Affiliated to JNTUK, Kakinada

Accredited by NAAC with "A" Grade, NBA (CSE, ECE, EEE, ME)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

List of Projects (Academic Year: 2018-19)

S.No	Project Title	Domain	Classification	Relevant to POs & PSOs
1	QOS Performance analysis of proactive reactive and hybrid routing protocols over fading channels	Communications	Research	PO1-PO12, PSO1,PSO2
2	Development of image analysis system by using convolution neural networks	Image Processing	Research	PO1-PO12, PSO1,PSO2
3	Developing side lobe reduction techniques using P-4 code for pulse compression Radar applications	Radar Signal Processing	Research	PO1-PO12, PSO1,PSO2
4	Design and development of shrafin antenna for vehicular communication applications	Antennas	Research	PO1-PO12, PSO1,PSO2
5	Design of PDP reusable FM0/Manchester encoder for DSRC applications	VLSI Design	Research	PO1-PO12, PSO1,PSO2
6	FPGA implementation of Radix-2 FFT architecture for twin data processor	VLSI Design	Research	PO1-PO12, PSO1,PSO2
7	Development of real time face detection and recognition system	Embedded Systems	Application	PO1-PO12, PSO1,PSO2
8	Some investigation on micro strip low pass filter and design approaches	Antennas	Research	PO1-PO12, PSO1,PSO2
9	Implementation of wireless sensor network node localization algorithm using MATLAB	Communications	Research	PO1-PO12, PSO1,PSO2
10	Design of earthquake alert system using Arduino and GSM module	Embedded Systems	Application	PO1-PO12, PSO1,PSO2
11	Design of multiband E-Shaped patch antenna with hexagonal slot for W-LAN applications	Antennas	Research	PO1-PO12, PSO1,PSO2

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12	Low light video enhancement using selective filters	Image Processing	Research	PO1-PO12, PSO1,PSO2
13	Implementation of fast multiplications by using unsigned quaternary number system	VLSI Design	Research	PO1-PO12, PSO1,PSO2
14	Design and implementation of low power and high-speed Braun multiplier using hybrid full adder	VLSI Design	Research	PO1-PO12, PSO1,PSO2
15	Designing of optimized energy DFlip-flop using inverse narrow width with pull-up /pull-down network	VLSI Design	Research	PO1-PO12, PSO1,PSO2
16	Haze removal using color attenuation prior	Image Processing	Research	PO1-PO12, PSO1,PSO2
17	Development of Quality Evaluation System for Fruits And Vegetables By Using Digital Image Processing Techniques	Image Processing	Research	PO1-PO12, PSO1,PSO2
18	CMOS Implementation of BaughWoolley And Wallace Tree Multiplier Architectures of Mac Unit	Embedded Systems	Application	PO1-PO12, PSO1,PSO2
19	Development of an Energy – Efficient System Using OFDMDAS Model For Wireless Applications	Communications	Research	PO1-PO12, PSO1,PSO2
20	Design of Reversible Gates – Based Image Steganography Using Quantum Dot Cellular Automata For Secure Nano Communication	VLSI Design	Research	PO1-PO12, PSO1,PSO2
21	Design of Serial Communication Based FFT Processor	Signal Processing	Research	PO1-PO12, PSO1,PSO2
22	Stair Shaped Di-Electric Resonator Antenna With Open-Ended Slot Ground For Wideband Applications	Antennas	Research	PO1-PO12, PSO1,PSO2

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23	Implementing An Energy Efficient Optimization For Base Stations in 5G Networks Using Particle Swarm Optimization	Communications	Research	PO1-PO12, PSO1, PSO2
24	Detection And Classification of Low Probability of Intercept Radar Signals Using Parallel Filter Arrays	Radar Signal Processing	Research	PO1-PO12, PSO1, PSO2
25	Design of Vedic Multiplier Architecture Using Adder Circuits	VLSI Design	Research	PO1-PO12, PSO1, PSO2
26	Design of 16 Bit Binary Multiplier Using Compressors	VLSI Design	Research	PO1-PO12, PSO1, PSO2
27	Enhancement of Low Light Images Using Local And Global Enhancement Methods	VLSI Design	Research	PO1-PO12, PSO1, PSO2
28	Multi Focus Image Fusion Through Multi Scale Morphological Focus Measure With Boundary Finding	Signal Processing	Research	PO1-PO12, PSO1, PSO2
29	Newly Proposed High Speed Multi out Carry Look-Ahead Adder	VLSI Design	Research	PO1-PO12, PSO1, PSO2
30	Design And Analysis of Hybrid Dielectric Resonator Antenna For Wideband And Multiband Applications	Antennas	Research	PO1-PO12, PSO1, PSO2
31	Implementation of arithmetic logic unit with TSPC D-Flip-flop using 0.13 μ m	VLSI Design	Research	PO1-PO12, PSO1, PSO2
32	Design of smart home using Internet of Things	IoT	Application	PO1-PO12, PSO1, PSO2
33	CMOS Implementation of array multiplier and serial-parallel multiplier architectures	VLSI Design	Research	PO1-PO12, PSO1, PSO2
34	Investigations on compact micro strip antenna for automotive communications	Antennas	Research	PO1-PO12, PSO1, PSO2
35	Design and analysis of UBW band pass filter using resonators	Antennas	Research	PO1-PO12, PSO1, PSO2
36	Smart plant health controlling systems	Embedded Systems	Application	PO1-PO12, PSO1, PSO2

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37	Design real coded Genetic Algorithm with location intelligence method for energy optimization in 5G networks	Communications	Research	PO1-PO12, PSO1,PSO2
38	Investigation on multilevel half rate phase detector for clock and data recovery circuits	VLSI Design	Research	PO1-PO12, PSO1,PSO2
39	Implementation power reduction in CMOS circuits	VLSI Design	Research	PO1-PO12, PSO1,PSO2
40	Design of hybrid full adders for power minimization and high-speed using XOR-XNOR gates	VLSI Design	Research	PO1-PO12, PSO1,PSO2
41	Development of MIMO-SVD based wireless sensor networks for improvement of channel capacity	Communications	Research	PO1-PO12, PSO1,PSO2
42	Design of smart wheel chair using hand gestures recognition	Embedded Systems	Application	PO1-PO12, PSO1,PSO2
43	Design of radix-4 based FFT processor using DSP slices	Signal Processing	Research	PO1-PO12, PSO1,PSO2
44	Recognition and de noising of QR CODE images using morphological operation	Image Processing	Research	PO1-PO12, PSO1,PSO2
45	IoT based garbage monitoring systems	IoT	Application	PO1-PO12, PSO1,PSO2
46	An improved design of approximate arithmetic units reversible logic gates for video encoding	VLSI Design	Research	PO1-PO12, PSO1,PSO2
47	Design and Development of secured bio-metric voting machine	Embedded Systems	Application	PO1-PO12, PSO1,PSO2


Project Coordinator


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